AMENDMENTS TO THE CLAIMS

1. (original) A delay locked loop for use in an integrated circuit device, comprising:

a coarse delay chain in series with a micro-stepped delay chain;

said course delay chain including a plurality of coarse delay units configured for selectively providing a coarse delay with respect to an input clock signal, and said micro-stepped delay chain configured for selectively providing a fine delay adjustment with respect to said input clock signal; and

said micro-stepped delay chain further comprising a plurality of parallel signal paths, wherein one or more of said parallel signal paths are capacitively loaded so as to provide said fine delay adjustment.

2. (original) The delay locked loop of claim 1, wherein:

a first of said plurality of parallel signal paths comprises a single coarse delay unit;

a second of said plurality of parallel signal paths comprises a pair of coarse delay units; and

the remainder of said plurality of parallel signal paths each comprising a single coarse delay unit having an intermediate node thereof loaded with a stepped value of capacitance with respect to one another;

wherein a signal propagated through any of said remainder of said plurality of parallel signal paths has a delay associated therewith that represents a stepped valued of delay between the delay provided by said single coarse delay unit and the delay provided by said pair of coarse delay units.

3. (original) The delay locked loop of claim 2, wherein said single coarse delay unit comprises a pair of serially connected NAND gates.

4. (original) The delay locked loop of claim 2, wherein:

an input signal to said micro-stepped delay chain is coupled to input terminals of each of said parallel signal paths; and

a micro-stepping control signal is coupled to said single coarse delay unit and said capacitively loaded single coarse delay units;

wherein said micro-stepping control signal is further configured such that only one of said single coarse delay unit and said capacitively loaded single coarse delay units are enabled at a given time.

5. (original) The delay locked loop of claim 4, wherein said micro-stepped delay chain further comprises an OR gate, said OR gate having each of said plurality of parallel signal paths as inputs thereto.

6. (original) The delay locked loop of claim 5, wherein said pair of coarse delay units is biased in an enabled state such that a maximum delay of a signal propagated through said micro-stepped delay chain is the delay provided by said pair of coarse delay units.

7. (original) The delay locked loop of claim 3, wherein said pair of serially connected NAND gates comprise equalized NAND gates.

8. (original) The delay locked loop of claim 1, wherein said coarse delay chain further comprises:

a plurality of serially connected coarse delay stages, each of said plurality of coarse delay stages configured to selectively provide a discrete number of coarse delay values, wherein the delay value of said discrete number of coarse delay values is successively larger for each successive coarse delay stage.

9. (original) The delay locked loop of claim 8, wherein said coarse delay stages

are configured such that discrete number of coarse delay values are implemented by routing an input signal through a specific number of said coarse delay units included within said coarse delay stages.

10. (original) The delay locked loop of claim 9, wherein said discrete number of coarse delay values are selected through a multiplexing device.

11. (original) The delay locked loop of claim 10, wherein at least a portion of said multiplexing device is configured from one of said coarse delay units.

12. (original) The delay locked loop of claim 9, wherein each of said coarse delay units comprises a pair of serially connected, NAND gates.

13. (original) The delay locked loop of claim 12, wherein said pair of serially connected NAND gates comprise equalized NAND gates.

14. (original) A micro-stepped delay chain for use in a delay locked loop, comprising:

a plurality of parallel signal paths coupled to a common input;

a first of said plurality of parallel signal paths comprising a single coarse delay unit;

a second of said plurality of parallel signal paths comprising a pair of coarse delay units; and

the remainder of said plurality of parallel signal paths each comprising a single coarse delay unit having an intermediate node thereof loaded with a stepped value of capacitance with respect to one another;

wherein a signal propagated through any of said remainder of said plurality of parallel signal paths has a delay associated therewith that represents a stepped valued of delay between the delay provided by said single coarse delay unit and the delay

provided by said pair of coarse delay units.

15. (original) The micro-stepped delay chain of claim 14, wherein each of said coarse delay units comprises a pair of serially connected NAND gates.

16. (original) The micro-stepped delay chain of claim 14, wherein:

a micro-stepping control signal is coupled to said single coarse delay unit and said capacitively loaded single coarse delay units;

wherein said micro-stepping control signal is further configured such that only one of said single coarse delay unit and said capacitively loaded single coarse delay units are enabled at a given time.

17. (original) The micro-stepped delay chain of claim 16, further comprising an OR gate, said OR gate having each of said plurality of parallel signal paths as inputs thereto.

18. (original) The micro-stepped delay chain of claim 17, wherein said pair of coarse delay units is biased in an enabled state such that a maximum delay of a signal propagated through the micro-stepped delay chain is the delay provided by said pair of coarse delay units.

19. (original) The micro-stepped delay chain of claim 17, wherein said pair of coarse delay units is biased in an enabled state such that a maximum delay of a signal propagated through the micro-stepped delay chain is the delay provided by said pair of coarse delay units.

20. (cancelled)